The paragraph beginning at page 7, line 21 of the specification as filed is amended as follows:

"In at least one embodiment of the present invention, as illustrated in Fig. 4, a slave-less edge-triggered flip flop 162 (e.g., flip flop 10 of Fig. 1, flip flop 60 of Fig. 2, etc.) is implemented within a digital processing device 164 (e.g., a microprocessor, a digital signal processor (DSP), a field programmable gate array (FPGA), a reduced instruction set computer (RISC), a complex instruction set computer (CISC), an application specific integrated circuit (ASIC), etc.) to serve as a data storage element within the device. The digital processing device 164 may be coupled to, for example, an external memory 166 (e.g., flash memory, dynamic random access memory (DRAM), static random access memory (SRAM), etc.) and/or other functionality to form a computing system 160. One or more slave-less edge-triggered flip flops may be used, for example, as an input/output data buffer for the digital processing device. Many alternative applications also exist."